

B. cont.
the frame memory is the same as or shorter than a remaining period, $M \cdot L - 3 \cdot L$, so that a speed of accessing said frame memory is less than $1/2$ of the data input speed.

16. A liquid crystal display comprising a memory controller according to claim 15.--

REMARKS

Claims 13-16 are now presented for examination. Claims 1-12 have been cancelled without prejudice. Claims 13-16 have been added to provide Applicants with a more complete scope of protection.

Claims 13 and 15 are the only independent claims.

Claims 1-12 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 4,745,485 (Iwasaki). First, cancellation of Claims 1-12 renders the rejection of those claims moot.

Claim 13 is directed to a memory controller that comprises: a serial/parallel converter section for converting bit width a (where a is a positive number) of an input data signal into a width N times ($N \geq 4$) as long as a ; a first FIFO memory of $a \cdot N$ bits in width for storing temporarily the signal after it has been subjected to the serial/parallel conversion; a frame memory having a capacity of a single frame for reading data at the same frequency as the input frequency of the input data after storing a predetermined quantity, $a \cdot N \cdot L$ bits (where L is an integer), of the data into the first FIFO memory, and for storing the data read out from the first FIFO memory; a memory controller for reading from and writing into the frame memory by driving successively as a single block; and a

second FIFO memory having width $a \cdot N$ for reading from the frame memory at the same frequency as the input data and for storing temporarily the data, such that, after storing data of a predetermined quantity $2 \cdot a \cdot N \cdot L$ into the second FIFO memory, the data is read at a frequency a half of the frequency of the input data. A continuous period of writing into and reading from the frame memory is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period NL , an instruction period (including latency) instructing the memory necessary for performing continuous access to the frame memory is the same as or shorter than a remaining period, $N \cdot L - 3 \cdot L$, so that a first FIFO size is set as $a \cdot N \cdot L$ bits, and a second FIFO size is set as $a \cdot N \cdot 2 \cdot L$ bits.

By virtue of the claimed structure, the frame rate of liquid crystal driving can be set twice as great as the frame rate of inputting an image. In Iwasaki, as understood, although the order of the input image and the order of liquid crystal displaying can be changed, the frame rate of the image input is the same as the frame rate of the liquid crystal driving. Kuwata discusses, at col. 4, lines 39-47, a Japanese publication that shows a memory controller used to reduce the memory capacity. However, in view of col. 5, lines 20-22, it is believed clear that using this memory control method, a memory having a capacity of two frames, i.e., one frame capacity for writing and one for reading, would be needed. In contrast, by virtue of the recited structure of the claimed invention, a memory of only one frame capacity is needed. Accordingly, new Claim 13 is believed patentable over the cited references. Independent Claim 15 recites similar features and is believed to be patentable for substantially similar reasons.

A review of the other art of record has failed to reveal anything which, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

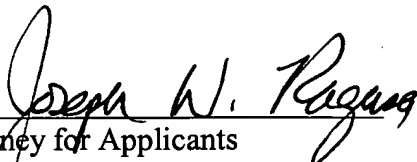
The other claims in this application are each dependent from one or the other of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of the patentability of each on its own merits is respectfully requested.

This Amendment After Final Rejection is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. At the very least, however, entry of this Amendment After Final Rejection, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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